LAW OFFICE OF
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## WHAT IS CLAIMED IS

1. A variable amplitude voltage regulator for use in a power factor correction system including in combination:

a resistor scaling network consisting of at least one variable resistor;

a source of rectified alternating current input voltage (ACR) coupled to the resistor scaling network;

a voltage error differential amplifier coupled to the ACR and to a reference signal to produce a voltage error signal (VES);

a digital signal processing (DSP) circuit;

means coupling the VES to the DSP to produce an output signal at a predetermined frequency with an adjustable duty ratio (DR);

means coupling the ACR and the output signal from the DSP to the resistor scaling network to produce a demand level control signal which varies as a function of the VES dc level.

2. The variable amplitude voltage regulator according to Claim 1 wherein the variable resistance comprises at least one bi-polar transistor having a base, an emitter, and a collector, the collector emitter path of which is connected in parallel with a fixed resistance with the collector emitter path supplied with the ACR, and the base supplied with the output signal from the DSP.

3. The variable amplitude voltage regulator according to Claim 2 wherein the predetermined frequency of the output signal of the DSP is a fixed frequency above the audible range and the transistor is switched fully on and off in a ratio determined by the adjustable duty ratio (DR) of the output of the DSP.

4. The variable amplitude voltage regulator according to Claim 3 wherein the demand level control signal (DLS) is defined by the following equation:

$$DLS = [(R1)/(R1+R2)] \times (1-DR) \times ACR$$

where R1 is the resistance of the transistor and R2 is the resistance of the resistor connected in parallel with the collector emitter path of the transistor.

5. The variable amplitude voltage regulator according to Claim 1 wherein the demand level control signal (DLS) is defined by the following equation:

$$DLS = [(R1)/(R1+R2)] \times (1-DR) \times ACR$$

where R1 is the resistance of the transistor and R2 is the resistance of the resistor connected in parallel with the collector emitter path of the transistor.

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